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A MULTIMODE INTERFACE ALLOWING TYPEWRITER OPERATION BY PARAPLEGICS (MITOP)

by

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A THESIS

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The undersigned certify that they have read, and recommended to the Faculty of Graduate Studies for acceptance, a thesis entitled A Multimode Interface allowing Typewriter Operation by Paraplegics, submitted by Richard Kildaw in partial fulfillment of the requirements for the degree of Master of Science.

ABSTRACT

This thesis deals with the design and construction of an interface which will allow physically handicapped people to communicate via a typewriter. Since many handicapped people, such as spastic and polio patients, are not able to communicate by ordinary means, this interface provides them with a method of expressing themselves.

The interface requires only a simple operation such as moving an arm, kicking a foot, blinking an eye, etc., to actuate a "switch". The first part of the switching sequence generated is translated into a position on a lightboard and the second part causes the function indicated on the lightboard to be typed on the typewriter. Control switches on the interface console are provided to preselect the mode and rate to be used in accessing and typing a desired function.

Many types of "switches", that plug into the interface, can be developed to accomodate a specific persons handicap. A combination of these "switches" and the multimode interface can be used to enable virtually all handicapped persons, with the knowledge of the language, to communicate via a typewriter.

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INTRODUCTION

The word interface means a surface forming a common boundary between two bodies and will in this case connote an electronic logic device that converts a sequence of simple actions into a more complex operation, that of typing a desired function. Such a device can be beneficially utilized by persons who can not communicate by ordinary means; but, can repeatedly perform some simple action.

In order to allow handicapped people to operate a typewriter by utilizing only the limited simple actions they are capable of performing, the interface must translate a sequence of simple actions into a desired function on the typewriter keyboard and then cause it to be typed. Secondly, it must provide some form of feedback to the operator to allow him to determine "where he is" in the sequence of simple actions and thereby determine the "next action" required to access and type the function desired.

Since the action each person can perform depends on his handicap, the interface was designed to respond to the two states of a switch. Various "switches" can then be designed to accomodate a specific persons handicap. The feedback mechanism developed, utilizes a visual display in the form of a lightboard. This lightboard consists of an arrangement of the typewriter keyboard functions superimposed on a matrix of lightbulbs that light up the background of only one function at a time. By supplying the

interface input with a certain switching sequence, the operator directs the interface to choose the desired function, as indicated on the lightboard, and then causes it to be typed. The form, sequence and number of simple actions required to access and type a desired function is controlled by the mode and selector switch positions on the console panel.

In order to make the interface versatile enough to accomodate many forms of handicaps, it was designed to operate in three modes.

In mode one, the operator locates the desired function on the lightboard by positioning a lever on the handboard with his arm. The function lit is then typed by actuating a "switch".

In mode two, the lightboard is continuously scanned at a rate set by the speed control on the console panel. When the desired function is lit, actuating a "switch" causes it to be typed.

In mode three, the operator controls the scanning of the lightboard by sequentially actuating his "switch". The first actuation causes the lightboard to be scanned horizontally from the "home position" (the upper left-hand square of the lightboard). The second actuation stops the horizontal scan and starts a vertical scan. The third actuation stops the scan at the desired function. The fourth actuation causes this function to be typed and returns the light to the "home position".

SYSTEM DESIGN CONSIDERATIONS

The main constraint on the overall design was the typewriter, an I.B.M. electric, model 868. This typewriter requires 60 millisecond pulses at >45 volts to operate the typewriter solenoids and is equipped with solenoids for only forty-seven keyboard operations.

Once the decision to use a lightboard as a visual aid was made, the size and number of the squares in the lightboard matrix posed another problem. It was found that 2½" matrix squares and a fairly high candlepower bulb were required to obtain sufficient resolution and contrast. An eight by eight lightboard matrix was chosen to allow some of the forty-seven typewriter functions to appear in more than one location, as well as to allow some simplification of the digital logic circuitry.

In view of the above, it was decided to have a 50 volt power source which would be:

(1) R-C filtered to supply the typewriter solenoids.

(2) R-C filtered and voltage divided to 28 volts to supply the lightbulbs used in the lightboard.

(3) R-C filtered and regulated to supply 40 volts to the photocell switches in the handboard. (one of the peripheral switch devices).

Economic and application considerations dictated the choice of Resistor Transistor Logic integrated circuitry for the logic requirements. This made the use of a 3.6 volt regulated supply necessary; therefore, it was decided to also have a 14 volt power source which would be:

(1) R-C filtered and regulated to supply 3.6 volts to the logic circuitry.

(2) R-C filtered to supply the bulb used to floodlight the photocells in the handboard.

Further decisions included:

(1) The use of Vector type boards and chassis for mounting and connecting the circuitry components, to facilitate the packaging of all power and logic components in one cabinet.

(2) The use of three modes, five speeds, four row sizes, and three column sizes, all selectable on the console panel to allow versatility and ease of operation.

SYSTEM OPERATION

A block diagram of the complete system is shown in FIGURE 1. The system consists of: the typewriter, the console, the lightboard, the handboard and the peripheral switch which are connected together by cables. The logic circuitry and switches of the console are broken into functional blocks, shown in FIGURE 2, for ease in describing their operation.

The matrix decoder sends information to the lightboard and the typewriter. It allows only one light at a time to be enabled on the lightboard. Column information varies the horizontal position of the light, and row information varies the vertical position. If the matrix decoder receives a pulse from the type pulser when a light is enabled, the function lit will be typed on the typewriter.

The mode switch on the console panel controls the mode of operation. In mode one operation, the matrix decoder takes information from the handboard via the mode controller. As the handboard position is varied it causes a horizontal scan of the lightboard. Row information is taken from the row converter which receives an increment signal from the handboard end stop via the mode controller. The type pulser is triggered by the peripheral switch via the mode controller.

In mode two operation, the matrix decoder takes

column and row information from the respective converters via the mode controller. Clock pulses increment the column converter causing a horizontal scan on the lightboard. Upon leaving the last position of a row, the end-row circuit increments the row converter and the horizontal scan continues one row down. Thus in this mode the lightboard matrix is continuously scanned. When the peripheral switch is actuated the mode controller inhibits the clock signal to the column converter, stopping the scan and at the same time triggers the type pulser causing the function lit to be typed. When the clock signal is enabled again, the scan continues. The rate of scan is preset by a five position switch on the console panel. The size of the matrix to be scanned can also be varied from eight by eight, to two by four, by the settings on the row and column switches on the console panel.

In mode three operation, the matrix decoder takes column and row information from the respective converters via the mode controller. Initially both converters are zeroed, causing the upper left-hand light on the lightboard to be lit. This is called the "home position". In this mode, the mode controller operates in a four signal cycle. Upon receiving the first signal from the switch circuit, the clock signal to the column converter is enabled. This causes a horizontal scan to begin. The second signal from the switch circuit inhibits the clock

signal to the column converter and enables the clock signal to the row converter; thereby, causing a vertical scan. The third signal from the switch circuit, inhibits the clock signal to the row converter and stops the scan. The fourth signal from the switch circuit triggers the type pulser. This causes the function lit to be typed and resets both row and column converters to zero. A fifth signal from the switch circuit acts the same as the first signal and a new cycle is started. Thus, in this mode the scan is under the control of the operator who determines when to switch in order to reach a desired function and cause it to be typed. The rate of scan can be preset as in mode two.

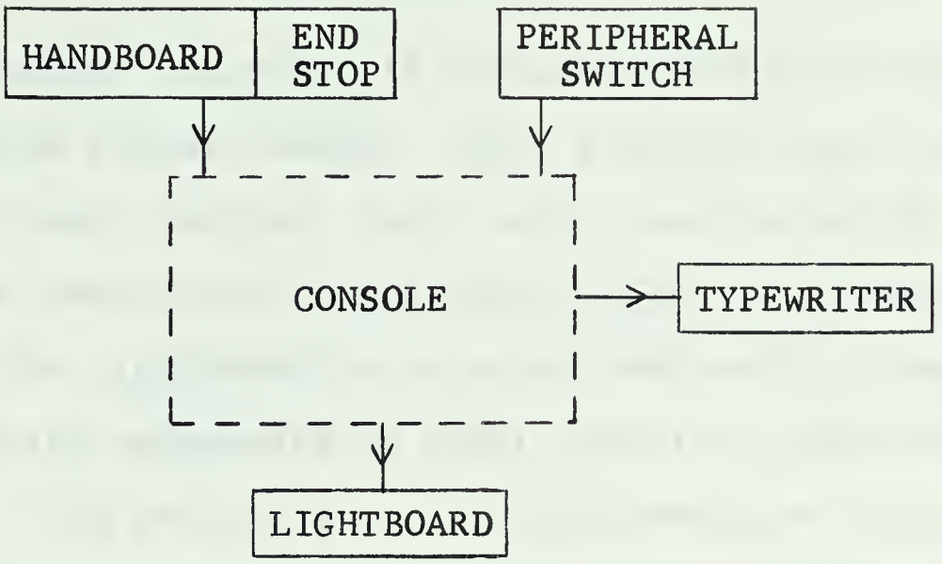


FIGURE 1 BLOCK DIAGRAM OF THE COMPLETE SYSTEM

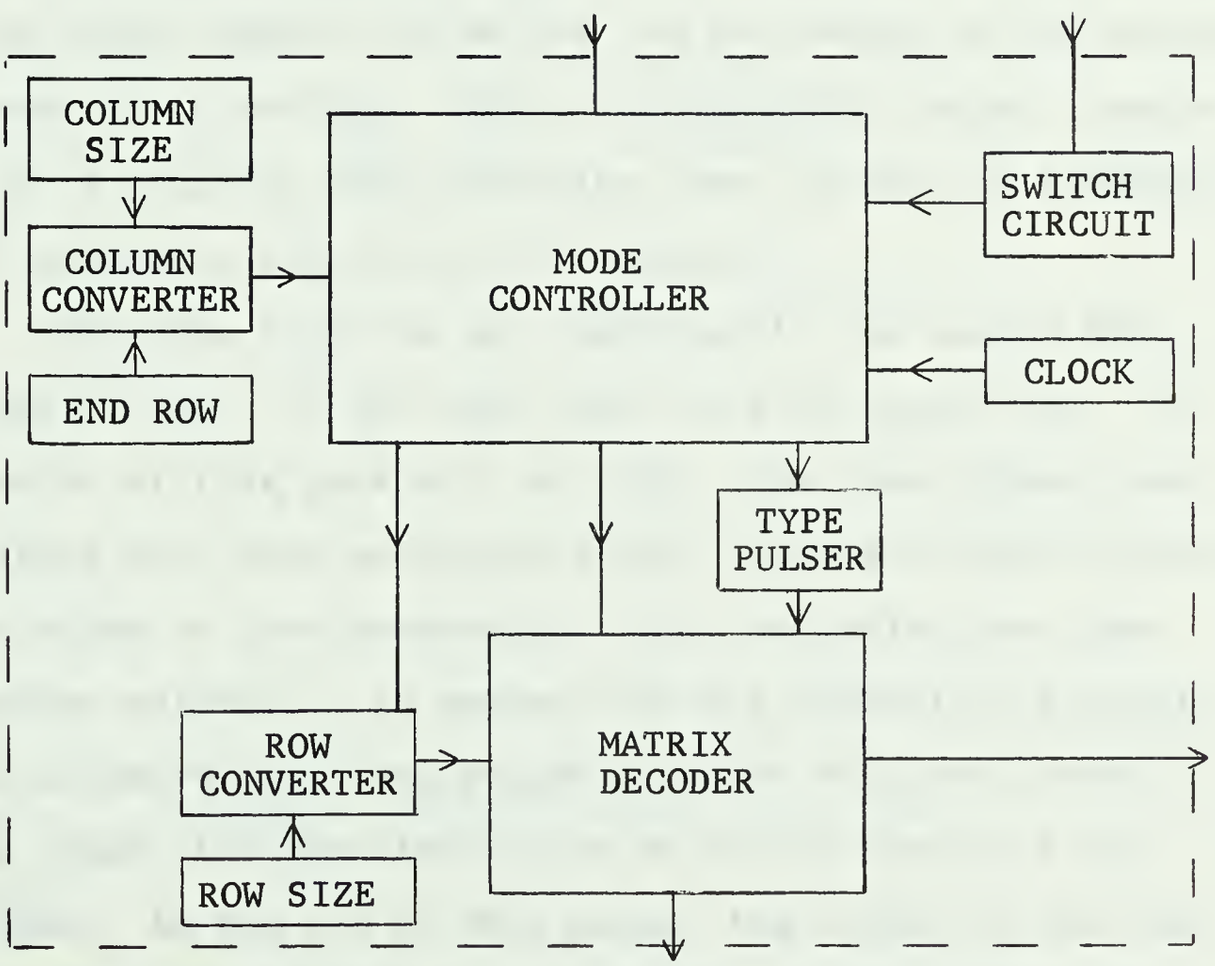


FIGURE 2 CONSOLE FUNCTIONAL BLOCK DIAGRAM

MATRIX DECODER

The decoder circuitry is contained on eight identical printed circuit boards. Each printed circuit board contains eight identical logic units, each of which represent one position on the eight by eight lightboard matrix. The lightboard is wired so that each printed circuit board represents an eight position column; thus, the sixty-four positions on the lightboard are obtained.

Each logic unit is connected as shown in FIGURE 3. When both column and row inputs to the first NOR gate are low, the output is high. This causes the output of the first inverter to be low and the output of the second inverter to be high. Thus, the lightbulb driver transistor is supplied with sufficient base current to cause it to saturate, and turn on the light.

When the light is on, one input to the second NOR gate is low. If the type input is also driven low, the output of this gate will go high. The type driver transistor will then be supplied with sufficient base current to drive it into saturation; thus, actuating the typewriter solenoid. To ensure that the typewriter solenoid is actuated just long enough to cause only one letter to be typed, the type input must be in the form of a low pulse. At the end of this pulse, the output of the second NOR gate returns to a low state. This causes the transistor to turn off and stop the current flow through

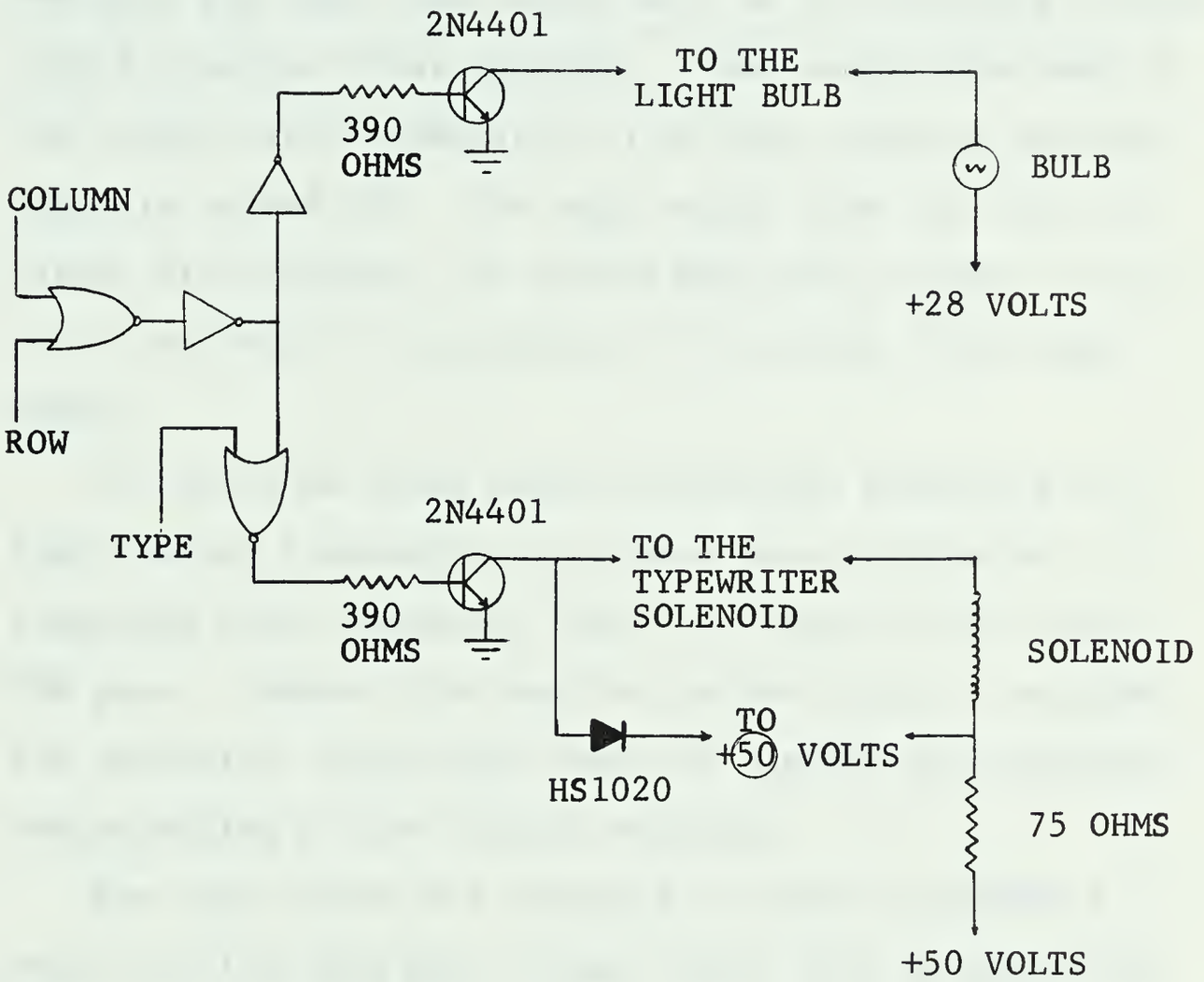


FIGURE 3 MATRIX DECODER LOGIC UNIT

the solenoid. The diode is used to de-energize this inductive solenoid circuit without exceeding the voltage rating of the transistor.

If either one, or both, of the inputs to the first NOR gate are high, its output will be low, causing a high output from the first inverter. This causes the base of the light driver transistor to be low, ensuring that the light is turned off. The high output from the first inverter also inhibits the second NOR gate causing its output to be held low regardless of the state of the type input.

It should be noted that the inverter supplying the light driver transistor could have been eliminated, by supplying this transistor from the output of the first NOR gate. However, the smaller series resistor required for operation, would have made the loading and therefore the switching of the circuit marginal.

The logic units are arranged as shown in FIGURE 4. Only the first NOR gate of each logic unit is shown for clarity.

If all column inputs (C1 to C8) except one are low, and all row inputs (R1 to R8) except one are high then only one light will be lit. For example if the inputs are:

C1	C2	C3	C4	C5	C6	C7	C8
0	0	1	0	0	0	0	0

and

R1	R2	R3	R4	R5	R6	R7	R8
1	1	1	0	1	1	1	1

only the light in the third column and the fourth row will be lit.

Note that all the type inputs can be triggered but only the function lit will be typed.

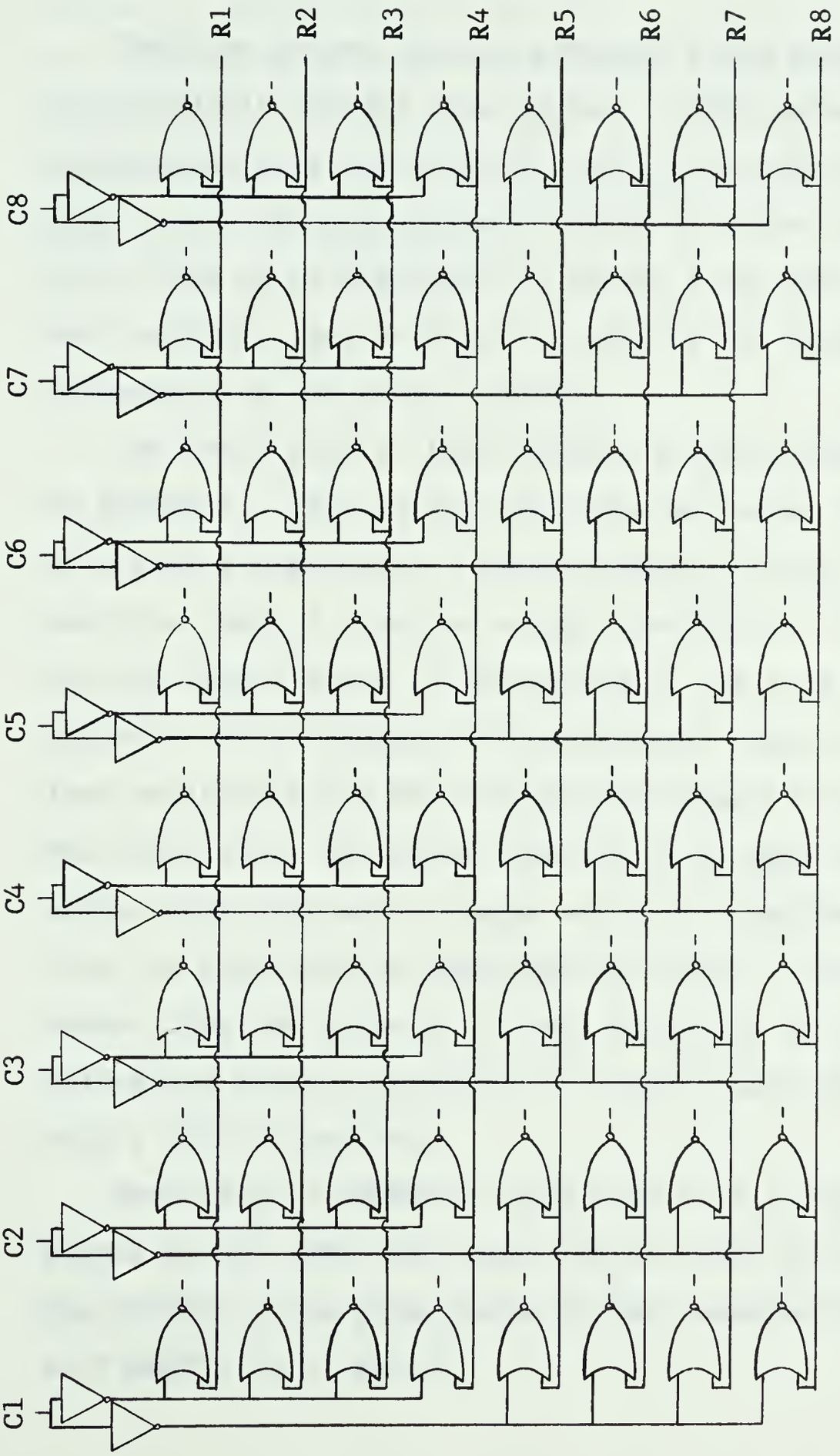


FIGURE 4 MATRIX DECODER

TYPE PULSER

The type pulser circuit provides a low going pulse to the matrix decoder type inputs. This pulse has a 60 millisecond duration which allows the typewriter to type only once. The type pulser circuit is shown in FIGURE 5. It is made up of NOR gates to obtain a one-shot with correct polarity, and buffered to satisfy the loading requirements of the matrix decoder.

The basic part of this circuit is the one-shot shown in FIGURE 6. This circuit provides an output consisting of a high going pulse of predetermined duration, only when the input X receives a high transition. The duration of this output pulse is determined by the size of the capacitor, the resistance of the inverter input, the B^+ feed resistance and the threshold voltage of the inverter. The duration of the pulse required to trigger the typewriter made necessary a large value of capacitance; therefore, an electrolytic capacitor was used. In order to ensure that the polarity of this capacitor is correctly maintained during operation, the gate output is loaded with a 220 ohm resistor.

Returning to FIGURE 5, note that only low going pulses at the INPUT can cause the one-shot to trigger and produce a low going pulse of the required duration at T DRIVE 1, 2, and 3.

Note also, that in order for a pulse at the INPUT to succeed in triggering the one-shot it must exceed the time constant made up by the 20 MFD. capacitor, the B^+ resistance of the first NOR gate and the input resistance of the second NOR gate. This arrangement sacrifices speed to gain noise immunity.

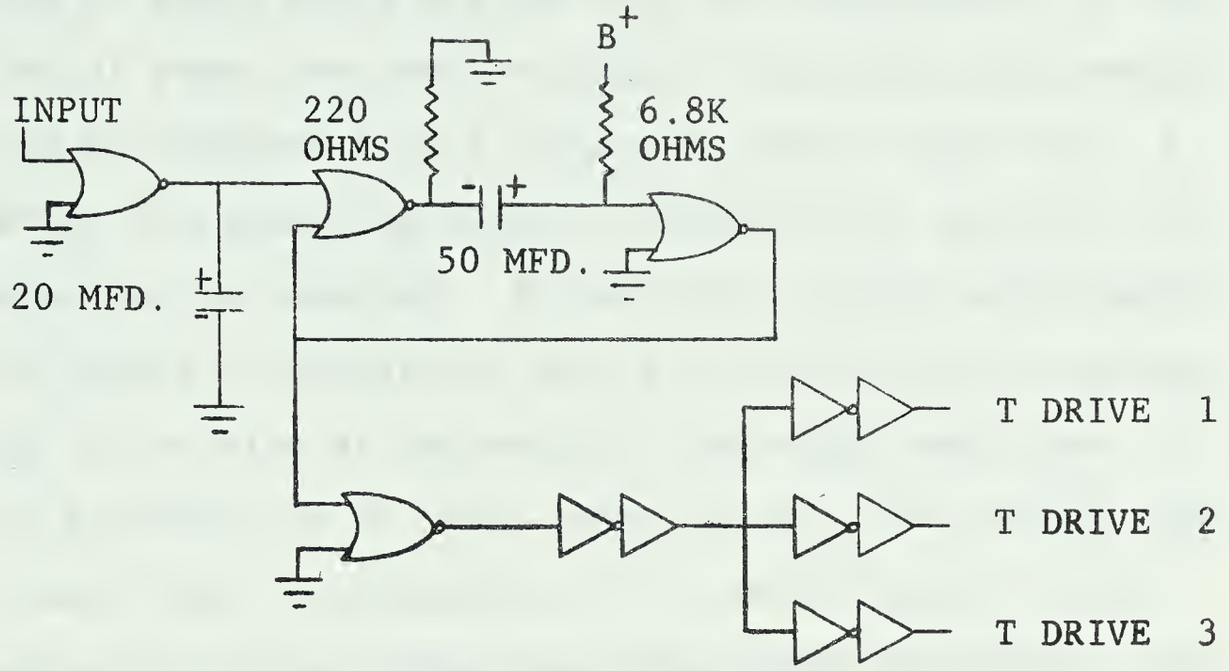


FIGURE 5 TYPE PULSER

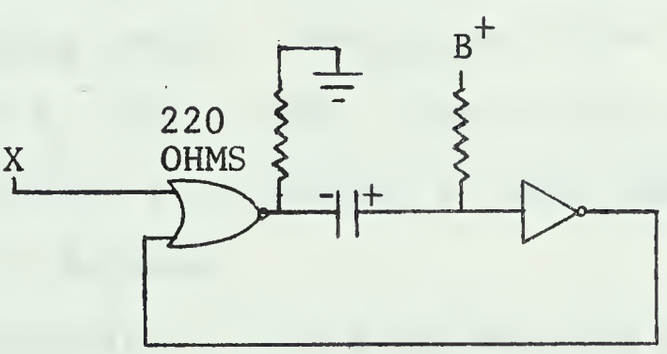


FIGURE 6 ONE-SHOT

SERIAL TO PARALLEL CONVERTER

The matrix decoder requires column information in the form of seven highs and one low; row information in the form of seven lows and one high. Since this information must be obtained from a series of simple operations, a method of converting serial information to parallel information is required. In addition to this requirement, the method of conversion must also facilitate the changing of the size of the matrix, from eight positions to two positions in at least steps of two. The method used to meet these requirements is to convert serial information to a binary code, and then decode the binary code into parallel information.

Since the maximum number count needed is eight, the binary code is generated by using three J-K flip-flops with additional circuitry to provide the appropriate combination of the S and C inputs to allow changing the size of the counting cycle. Conversion of the binary code is accomplished by using eight, three input gates whose outputs are buffered as necessary to meet the requirements of the matrix decoder.

Row information in the form required by the matrix decoder is obtained by using the binary coded outputs and their complements as shown in FIGURE 7. Likewise, column information is obtained as shown in FIGURE 8.

INPUT			OUTPUT								CIRCUIT
A	B	C	R1	R2	R3	R4	R5	R6	R7	R8	
0	0	0	0	1	1	1	1	1	1	1	
0	0	1	1	0	1	1	1	1	1	1	
0	1	0	1	1	0	1	1	1	1	1	
0	1	1	1	1	1	0	1	1	1	1	
1	0	0	1	1	1	1	0	1	1	1	
1	0	1	1	1	1	1	1	0	1	1	
1	1	0	1	1	1	1	1	1	0	1	
1	1	1	1	1	1	1	1	1	1	0	

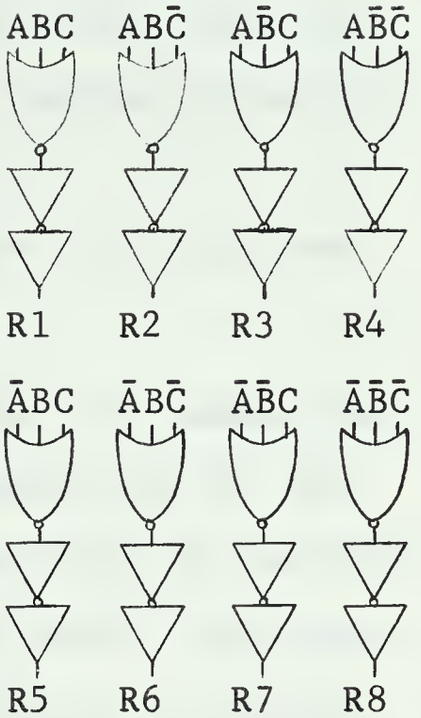


FIGURE 7 BINARY TO PARALLEL ROW CONVERTER

INPUT			OUTPUT								CIRCUIT
A	B	C	C1	C2	C3	C4	C5	C6	C7	C8	
0	0	0	1	0	0	0	0	0	0	0	
0	0	1	0	1	0	0	0	0	0	0	
0	1	0	0	0	1	0	0	0	0	0	
0	1	1	0	0	0	1	0	0	0	0	
1	0	0	0	0	0	0	1	0	0	0	
1	0	1	0	0	0	0	0	1	0	0	
1	1	0	0	0	0	0	0	0	1	0	
1	1	1	0	0	0	0	0	0	0	1	

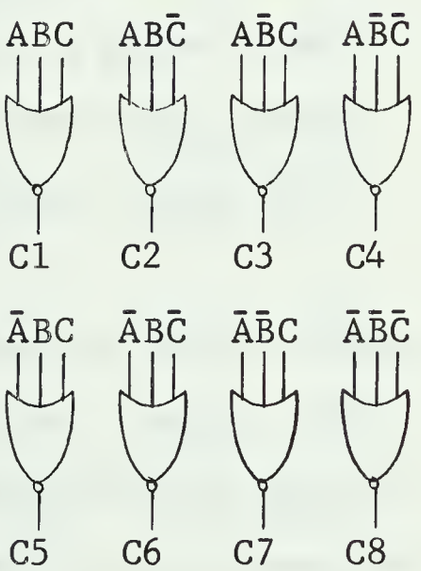


FIGURE 8 BINARY TO PARALLEL COLUMN CONVERTER

When a binary counting sequence is applied to the input of the binary to parallel row (column) converter, it causes the row (column) outputs to enable the matrix decoder rows (columns) in sequence.

The characteristic equation for the J-K flip-flops used is: $$Q_{n+1} = S \cdot Q_n + \bar{C} \cdot \bar{Q}_n$$

where n refers to the state of the flip-flop immediately preceding a dynamic zero (a 1 to 0 transition) at the toggle input and the n+1 refers to the state of the flip-flop immediately following the dynamic zero. This property of the J-K flip-flop makes it amenable to application in sequential configurations that utilize synchronous toggling of the flip-flops.

The required binary counters were designed using Karnaugh map techniques which yield the S and C input requirements for each flip-flop used in a given count cycle. FIGURES 9, 10, 11 and 12 illustrate the method used and the solutions obtained for count cycles of 8, 6, 4 and 2 counts respectively.

The counting cycle used for the smaller matrix sizes is centered around the binary 011 and 100 states. This allows the change of state of the A flip-flop to be utilized in mode two operation to trigger the row converter each time the column converter is re-cycled.

Since redundant states occur in the 2, 4 and 6 cycle counters, there are a number of signals that could be

used for the S and C inputs. Therefore, the signals were selected to minimize the number of different inputs required; thereby, minimizing the number of pins needed on the Vector boards. This required that the flip-flops be cleared between each change in size of the count cycle. To accomplish this clearing operation the preclear input to each flip-flop must be pulsed high. By using the fact that the matrix size selector switches are of the non-shorting type, their open time during switching is used via an inverter to provide the preclear pulse.

STATE				KARNAUGH MAPS	EQUATIONS
$A_nB_nC_n$	A_{n+1}	B_{n+1}	C_{n+1}		
0 0 0	0	0	1	A_{n+1}	$(\overline{C}+\overline{B})A+(B\cdot C)\overline{A}$
0 0 1	0	1	0		$(\overline{B\cdot C})A+(\overline{B\cdot C})\overline{A}$
0 1 0	0	1	1		$S_A=\overline{B\cdot C}$ $C_A=\overline{B\cdot C}$
0 1 1	1	0	0	B_{n+1}	$(\overline{C})B+(C)\overline{B}$
1 0 0	1	0	1		$(\overline{C})B+(\overline{C})\overline{B}$
1 0 1	1	1	0		$S_B=\overline{C}$ $C_B=\overline{C}$
1 1 0	1	1	1	C_{n+1}	$(0)C+(1)\overline{C}$
1 1 1	0	0	0		$(0)C+(\overline{1})\overline{C}$
					$S_C=0$ $C_C=0$

FIGURE 9 EIGHT COUNT CYCLE CODING

STATE						KARNAUGH MAPS	EQUATIONS
A_n	B_n	C_n	A_{n+1}	B_{n+1}	C_{n+1}		
0	0	0	0	0	1	A_{n+1}	$(\overline{B})A+(B\cdot C)\overline{A}$
0	0	1	0	1	0		$(\overline{B})A+\overline{(B\cdot C)}\,\overline{A}$
0	1	0	0	1	1	B_{n+1}	$(\overline{A}\cdot\overline{C})B+(C)\overline{B}$
0	1	1	1	0	0		$(\overline{A}\cdot\overline{C})B+\overline{(C)}\,\overline{B}$
1	0	0	1	0	1	$S_B=\overline{A}\cdot\overline{C}$ $C_B=\overline{C}$	
1	0	1	1	1	0	C_{n+1}	$(0)C+(1)\overline{C}$
1	1	0	0	0	1		$(0)C+\overline{(1)}\,\overline{C}$
						$S_C=0$ $C_C=0$	

FIGURE 10 SIX COUNT CYCLE CODING

STATE						KARNAUGH MAPS	EQUATIONS
A_n	B_n	C_n	A_{n+1}	B_{n+1}	C_{n+1}		
0	0	0	0	0	1	A_{n+1}	$(\overline{C})A+(B\cdot C)\overline{A}$
0	0	1	0	1	0		$(\overline{C})A+\overline{(B\cdot C)}\,\overline{A}$
0	1	0	0	1	1	B_{n+1}	$(\overline{A}\cdot\overline{C})B+(C)\overline{B}$
0	1	1	1	0	0		$(\overline{A}\cdot\overline{C})B+\overline{(C)}\,\overline{B}$
1	0	0	1	0	1	$S_B=\overline{A}\cdot\overline{C}$ $C_B=\overline{C}$	
1	0	1	0	1	0	C_{n+1}	$(0)C+(1)\overline{C}$
							$(0)C+\overline{(1)}\,\overline{C}$
						$S_C=0$ $C_C=0$	

FIGURE 11 FOUR COUNT CYCLE CODING

STATE						KARNAUGH MAPS	EQUATIONS
A_n	B_n	C_n	A_{n+1}	B_{n+1}	C_{n+1}		
0	0	0	0	1	1	A_{n+1}	$(0)A+(B\cdot C)\overline{A}$
0	1	1	1	0	0		$S_A=0 \quad C_A=\overline{B\cdot C}$
1	0	0	0	1	1	B_{n+1}	$(0)B+(1)\overline{B}$
							$S_B=0 \quad C_B=0$
						C_{n+1}	$(0)C+(1)\overline{C}$
							$S_C=0 \quad C_C=0$

FIGURE 12 TWO COUNT CYCLE CODING

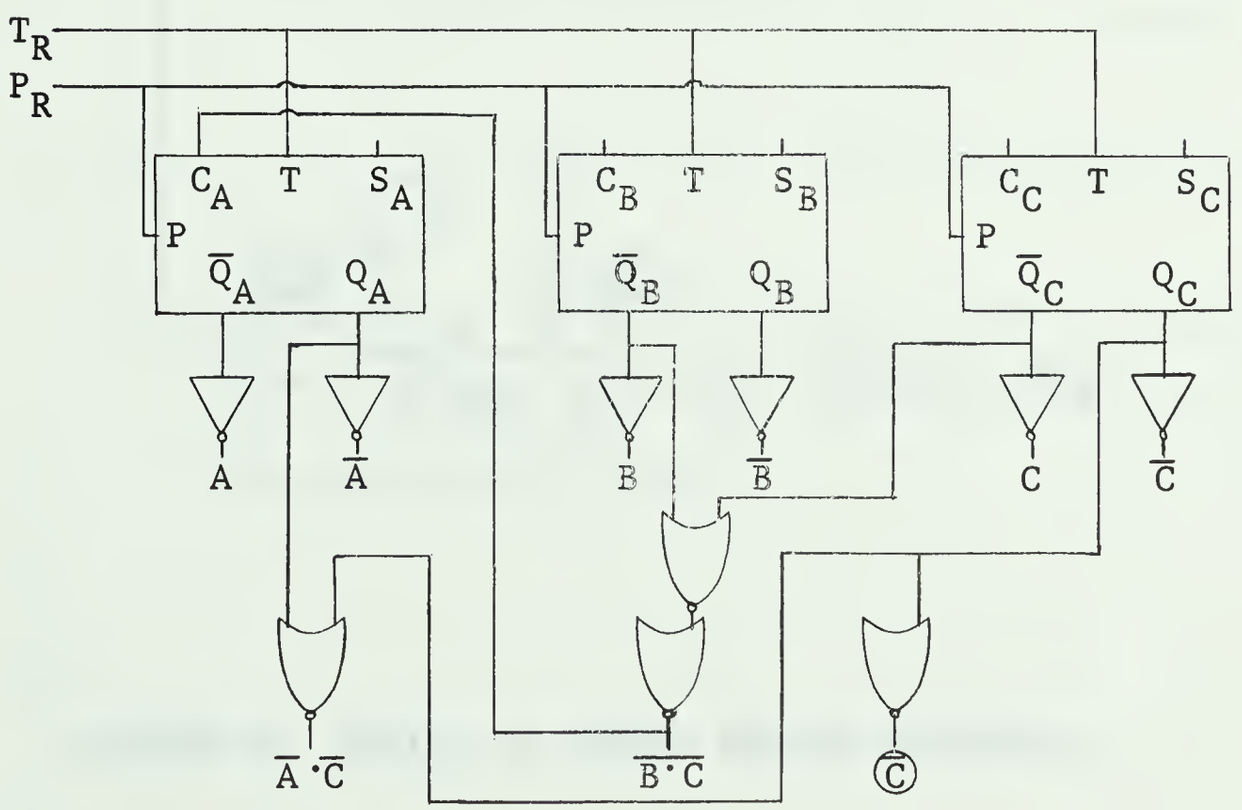


FIGURE 13 SERIAL TO BINARY ROW CONVERTER

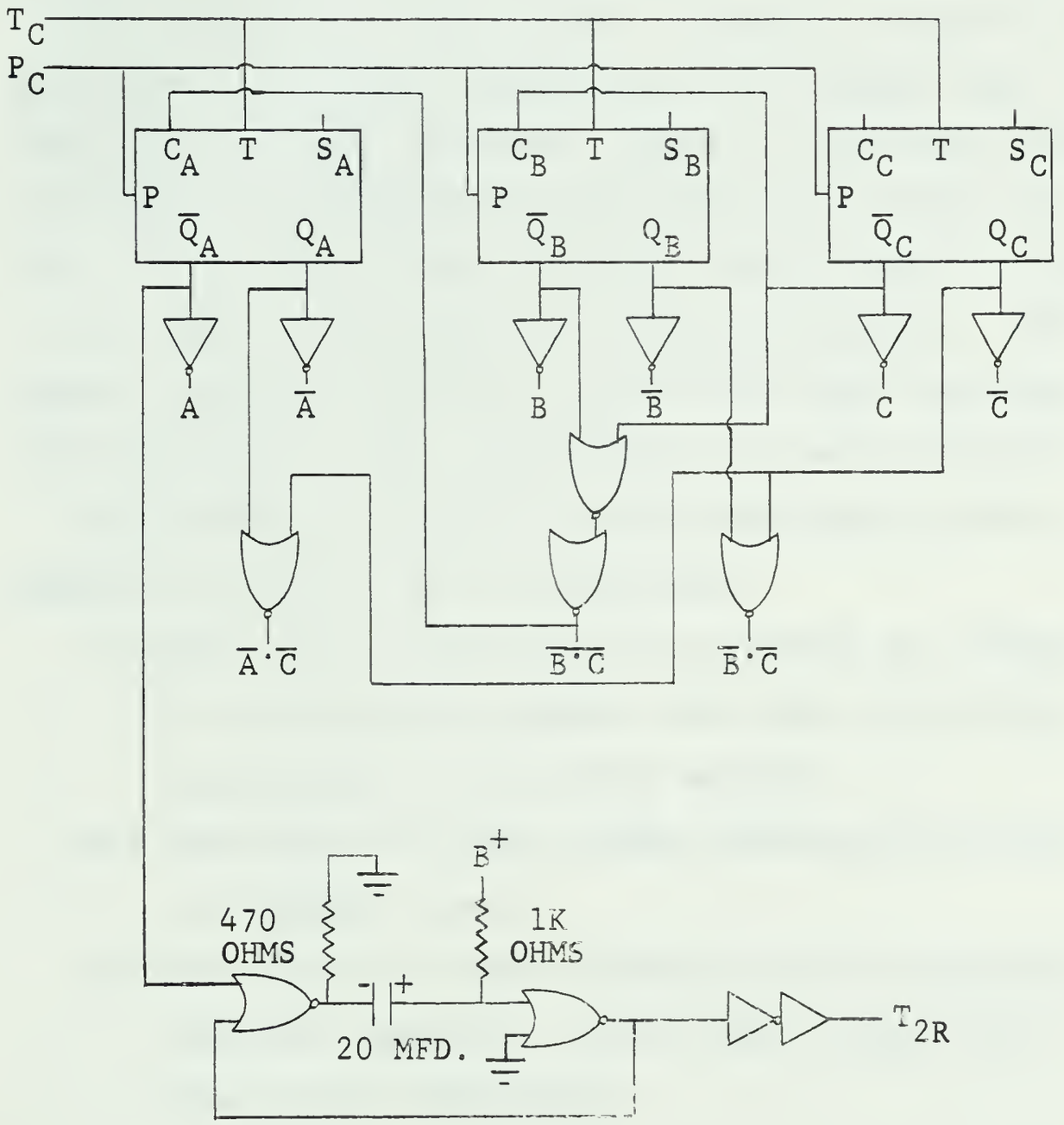


FIGURE 14 SERIAL TO BINARY COLUMN CONVERTER

FIGURE 13 is the schematic for the serial to binary row converter and FIGURE 14 is the schematic for the serial to binary column converter.

The operation of each serial to parallel converter is as follows: Low going transitions at the toggle input of the serial to binary converter, cause its flip-flop states to change in the sequence dictated by their S and C inputs. This change in the flip-flop states causes a change in the output of the binary to parallel converter. The binary to parallel converter outputs are then translated into a position on the lightboard by the matrix decoder.

The differences between the row and column serial to parallel converters are outlined below:

(1) The output of the binary to parallel row converter is buffered to satisfy the logic and loading requirements of the matrix decoder.

(2) The serial to binary column converter has an end-row trigger circuit.

(3) The serial to binary converters use an optionally different coding for their S and C inputs due to count cycle differences.

MODE CONTROLLER

The mode controller conditions information from the handboard, the switch circuit and the clock. It then directs this and other information to the converters, the type pulser and the matrix decoder; via a twenty one pole, three position mode switch. A mechanical switch was used for this purpose because of space and cost considerations.

In mode one, the matrix decoder receives column information from the handboard. The handboard end stop signal is applied to T_{IN} shown in FIGURE 15A. A low going transition of the end stop signal causes a low pulse to be generated at T_{OUT}. T_{OUT} is connected to the input of the row converter which causes the matrix decoder to advance the light one row. The normally high output, OUT, from the switch circuit is connected to the type pulser and causes it to generate a type pulse each time the switch circuit is actuated.

In mode two, the row and column converters are connected to the matrix decoder. The clock is connected to the column converter and the end-row circuit is connected to the row converter. The clock continuously increments the column converter causing a horizontal scan of the lightboard, and the end-row circuit increments the row converter each time the column converter is re-cycled. Thus, the lightboard is scanned continuously.

In order to facilitate the typing of a function reached during the scan, the clock is switched to the column converter input as shown in FIGURE 15C. The normally high output, OUT, from the switch circuit is connected to the type pulser and the normally low output, $\overline{\text{OUT}}$, is connected to the preclear input of the flip-flop. The flip-flop scheme used operates as follows: a high signal on the preclear input clamps the output low, inhibiting the clock from changing the state of the flip-flop. After the high preclear signal has changed to a low, each dynamic zero of the clock causes the state of the flip-flop to change. The operation sequence shown in FIGURE 16 illustrates this.

From the circuit shown in FIGURE 15C, it can be seen that when the switch circuit is actuated, the preclear input goes high and the type pulser input goes low. This causes T DRIVE 3 to go low for the duration of the type pulse. Thus, the NOR gate is inhibited by either V or $\overline{\text{T DRIVE 3}}$ until both the type pulse is finished and a low clock transition is allowed to change the state of the flip-flop. This means that T_{2C} is held high and the scan is stopped until typing and de-actuation of the switch circuit are completed. FIGURE 17 illustrates this operation sequence. The use of this flip-flop scheme ensures that the scanning light remains in the position next to the one typed, for the full period of one scan pulse.

In mode three operation the mode switch connects: the row and column converters to the matrix decoder, T_{3R} to the row converter input, T_{3C} to the column converter input, TYPE 3 to the type pulser input, $\overline{\text{T DRIVE 3}}$ to T_{IN}, as well as $P_C P_R$ to the preclear inputs of the row and column converters via inverters.

The schematic is shown in FIGURE 15B, and FIGURE 18 illustrates one operation sequence. Switching into mode three preclears all the flip-flops. Thus, initially T_{3R} and T_{3C} are held high and TYPE 3 is held low. Actuating the switch circuit causes OUT to go low and $\overline{\text{OUT}}$ to go high. The low transition of OUT causes d12 and b12 to go low allowing CLOCK X to produce a clocked output at T_{3C}. This in turn, causes a horizontal scan of the lightboard. De-actuating the switch circuit causes d12 to go high, this holds T_{3C} high and stops the horizontal scan. At the same time $\overline{\text{OUT}}$ goes low, causing d10 and b10 to go low. This allows CLOCK X to produce a clocked output at T_{3R}, and thereby starts a vertical scan on the lightboard. Actuating the switch circuit for the second time causes d12 to go low; but, at the same time d13 is driven high. Thus, T_{3C} remains high. This actuation also causes d10 to go high, which drives T_{3R} high and stops the scan. De-actuation of the switch circuit now causes d10 to go low; but, at the same time d9 is driven high. Thus, T_{3R} remains high. This de-actuation also causes d6 and d7 to

go low, which in turn causes a low transition at TYPE 3. This transition is used to trigger the type pulser. The trailing edge of the type pulse produced is used to supply T_{IN} with a low transition. This in turn, generates a pulse that preclears all the flip-flops. The cycle is now ready to be repeated.

The arrangement of flip-flops ensures that the time spent in each position, where switching does not take place, is of equal duration. The inverters and capacitors in the OUT and $\overline{\text{OUT}}$ leads to d12 and d10 respectively, delay the transition of these signals by approximately the same time as the signal delay through the flip-flops. Many schemes can be used to perform this operation and more than one controller was designed and built. However, this design yields good results with a reasonable number of components.

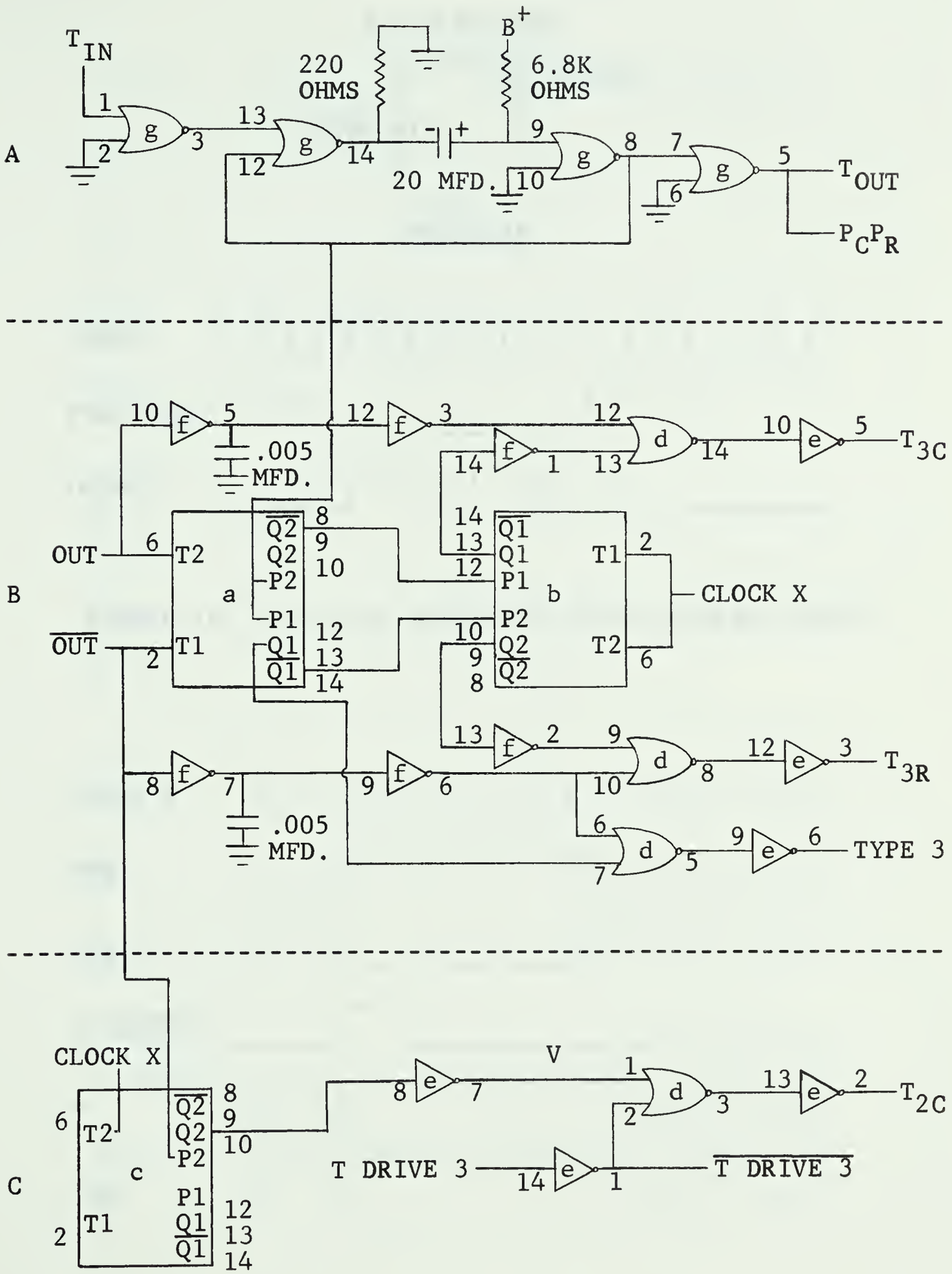
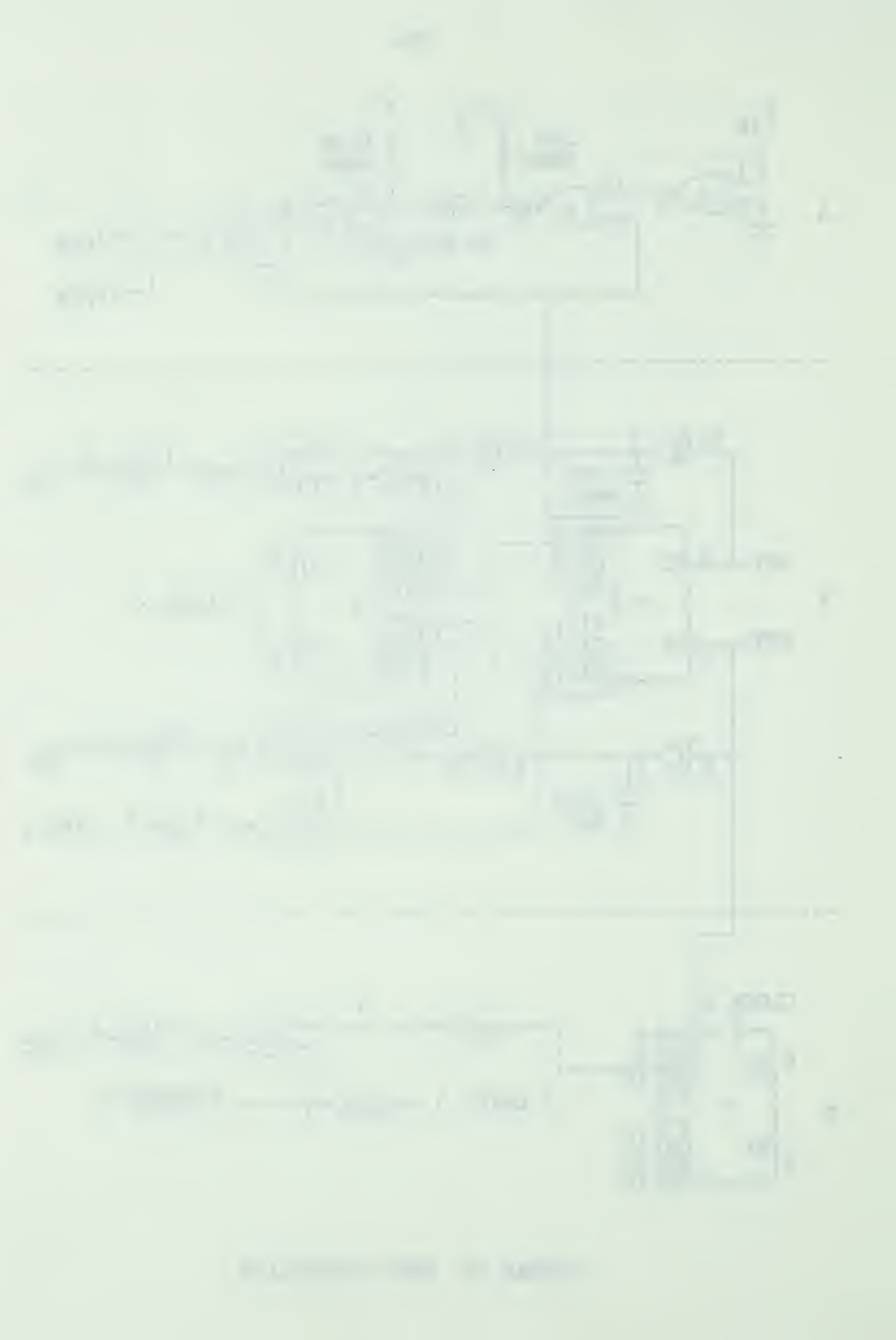


FIGURE 15 MODE CONTROLLER



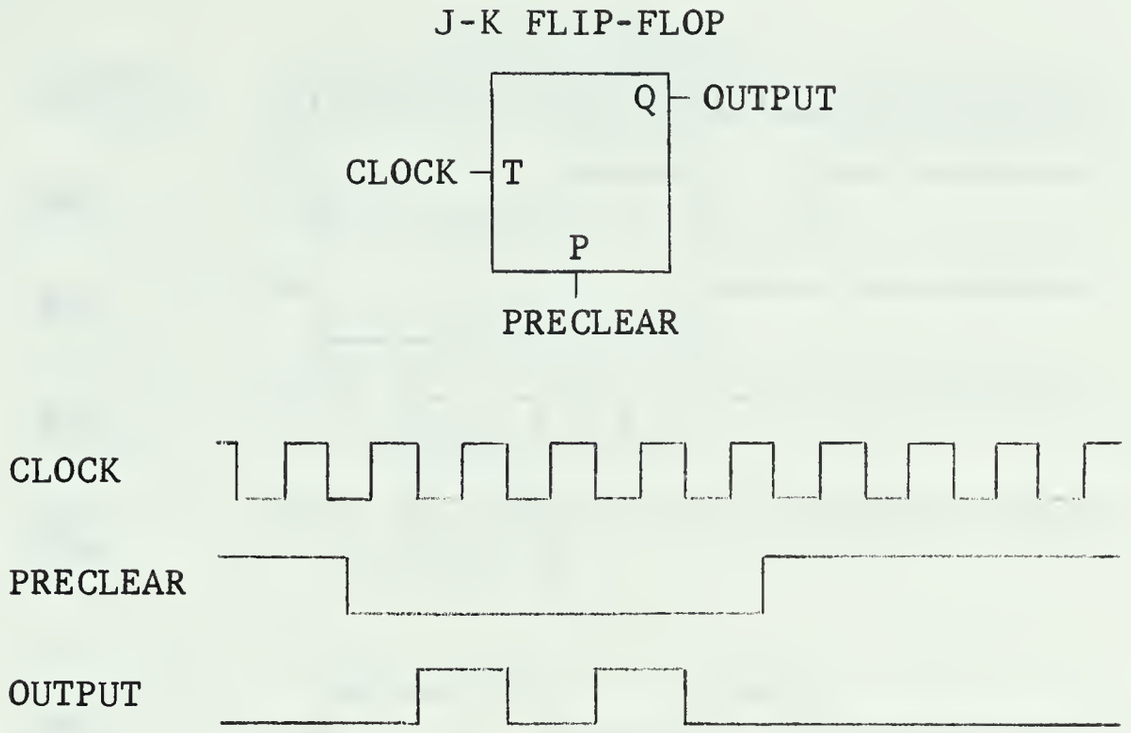


FIGURE 16 FLIP-FLOP OPERATION USING PRECLEAR INPUT

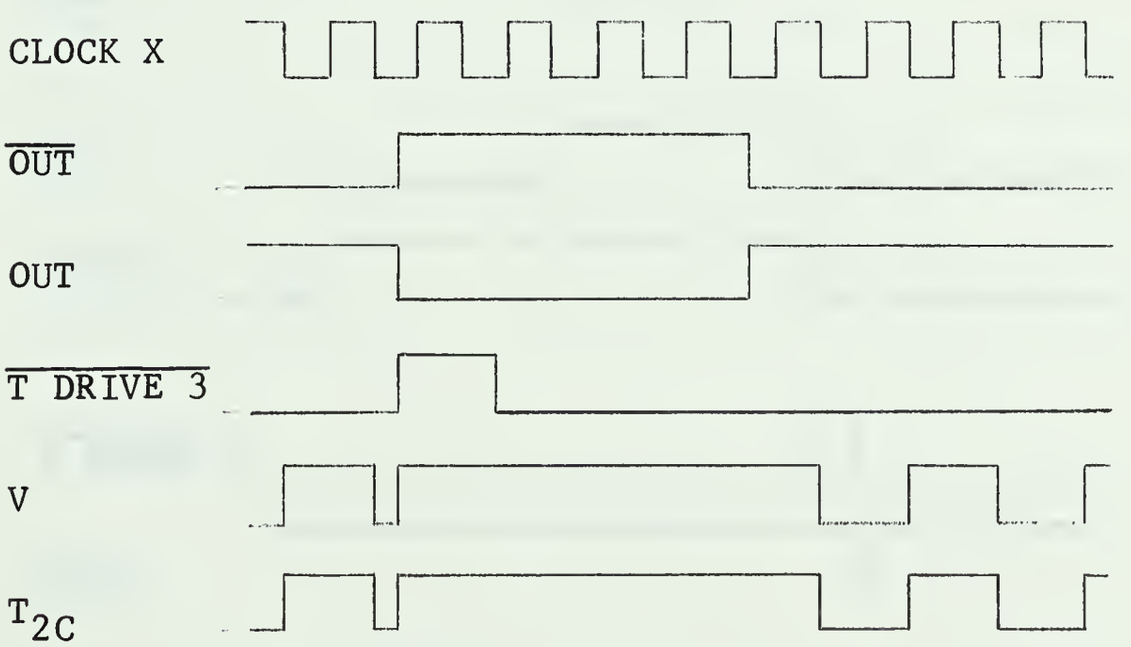


FIGURE 17 MODE TWO OPERATION SEQUENCE

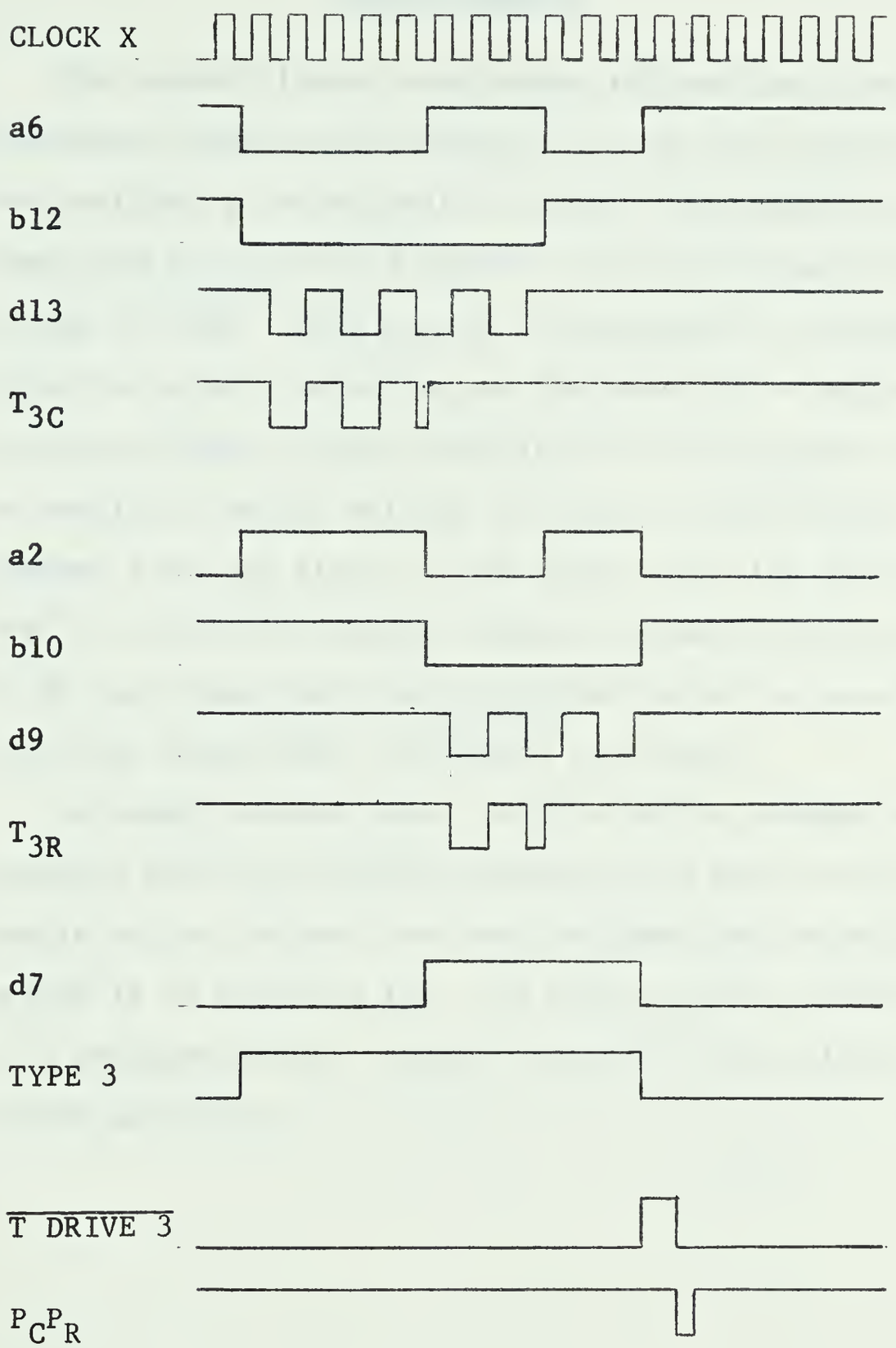


FIGURE 18 MODE THREE OPERATION SEQUENCE

SWITCH CIRCUIT

The switch circuit conditions information from a peripheral switch and directs it to the mode controller. Any peripheral switch which presents information in the same form as the set of N/C-N/O contacts shown in FIGURE 19 can be used. This switch is connected to no-bounce circuits; which, depending on the mode and selector switch settings, causes the switch circuit outputs to be single or double acting. (A single acting output changes from one state to the other each time the peripheral is closed and opened; while, a double acting output is in one state when the peripheral switch is open and the other state when the switch is closed)

In modes two and three, single acting outputs are produced when the selector switch is in position one and double acting outputs are produced when the selector switch is in position two. In mode one, the switch circuit produces double acting outputs in both selector switch positions.

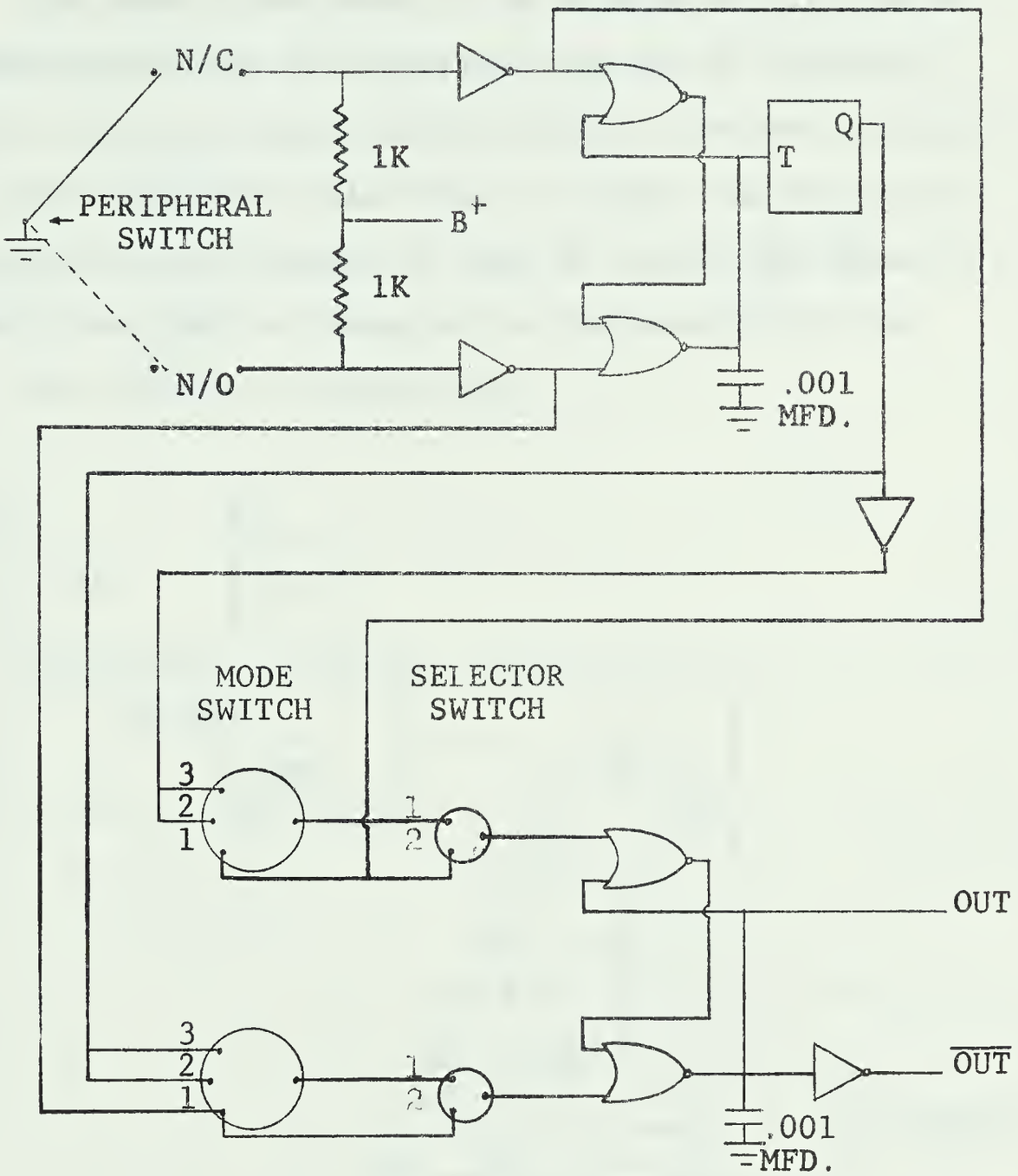


FIGURE 19 SWITCH CIRCUIT

CLOCK

The basic clock unit is an astable multivibrator, constructed from two inverters and two R-C networks. Its output is passed through another inverter and used to drive cascaded flip-flops to reduce the frequency. A five position switch is used to select the speed of the clock that is connected to the mode controller.

The circuit is shown below.

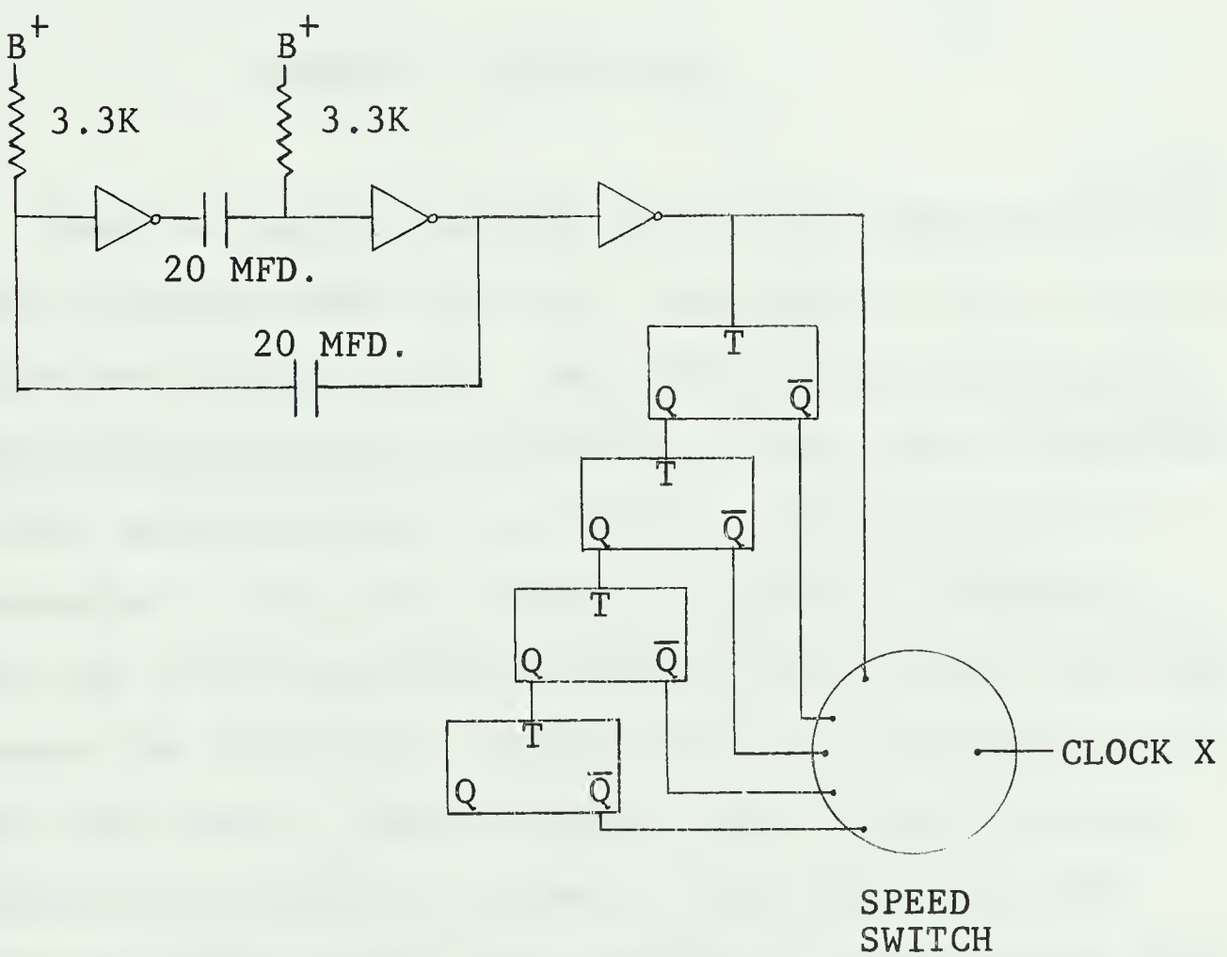


FIGURE 20 CLOCK CIRCUIT

SHIFT CIRCUIT

One of the positions on the lightboard is used to determine upper or lower case as shown.

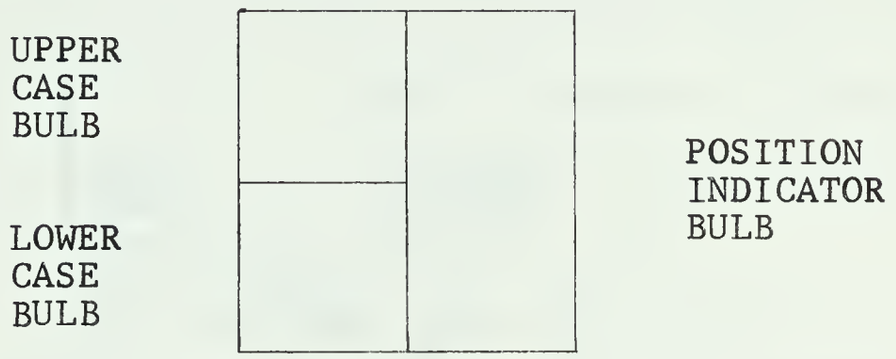


FIGURE 21 SHIFT CELL

When the upper case bulb is on, all functions are in upper case and when the lower case bulb is lit, all functions are in lower case. When the position bulb is lit, and the type pulser is actuated, a type driver transistor in the matrix decoder is pulsed on. This transistor is connected to the shift circuit as shown in FIGURE 22. The end of the type pulse triggers the one-shot shown and causes the flip-flop to switch off the bulb which was on, and vice versa. When the upper case bulb is lit, this circuit also supplies current to the typewriter shift solenoid which latches the typewriter in upper case until the type pulser is actuated in this position again.

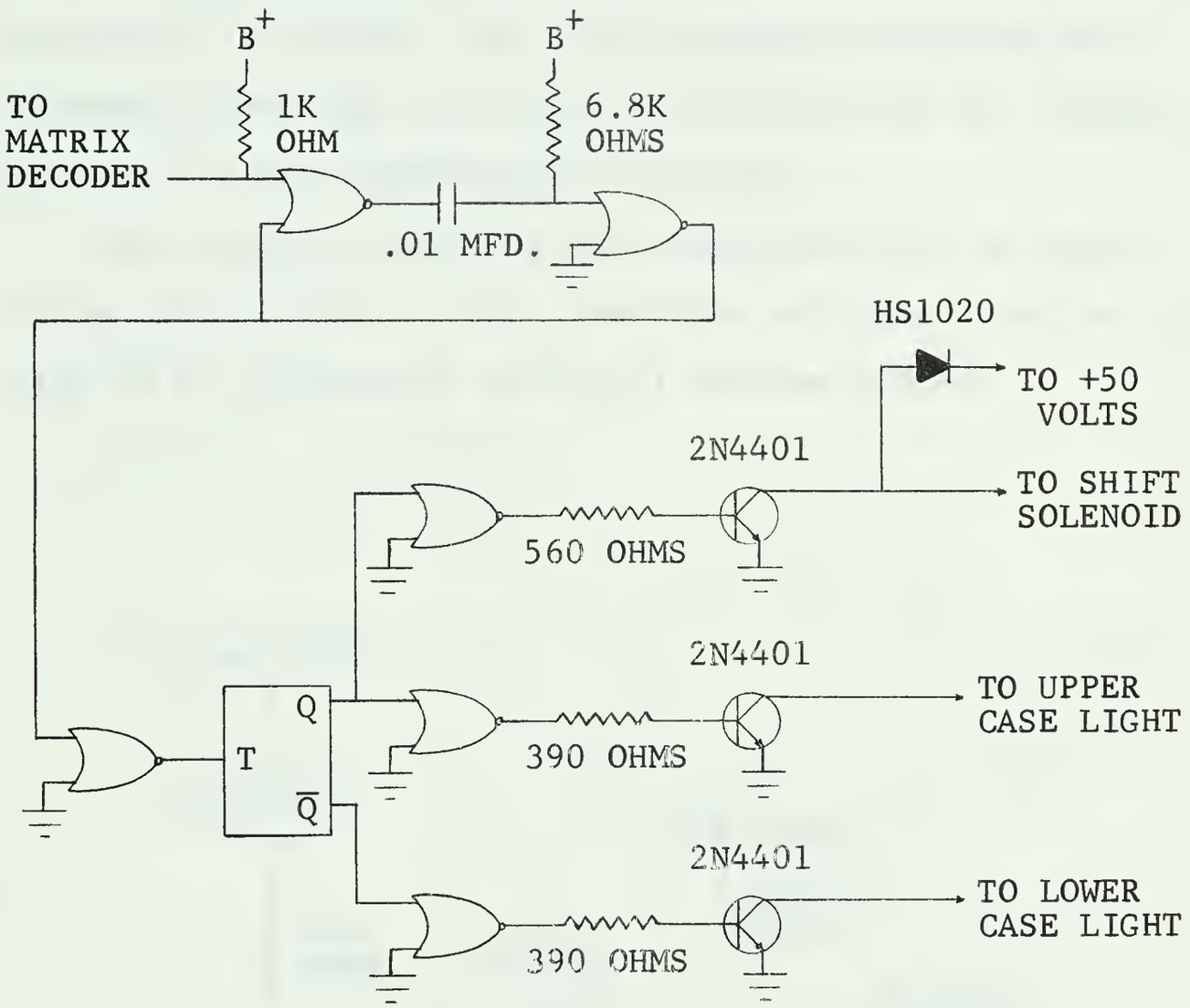


FIGURE 22 SHIFT CIRCUIT

HANDBOARD CIRCUIT

The handboard has seven photocells, which are spaced so that only one at a time can be shaded from a light source. A movement of $\pm 9^{\circ}$ is required before a different photocell is shaded. Thus, even imprecise motions can succeed in shading a photocell such that only the desired position on the lightboard is selected.

The circuit associated with each photocell is shown below. The output of the transistor switches from low to high as an illuminated photocell becomes shaded.

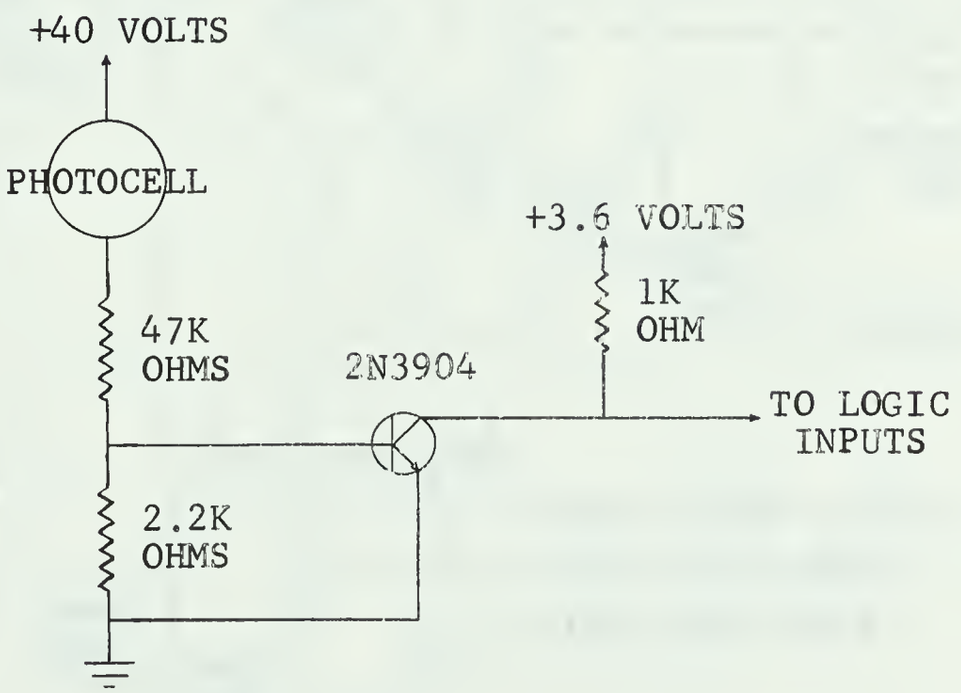


FIGURE 23 PHOTOCELL SWITCH UNIT

POWER SUPPLIES

Two transformers are used to obtain the required source voltages. Each voltage source is then full-wave rectified and filtered as shown.

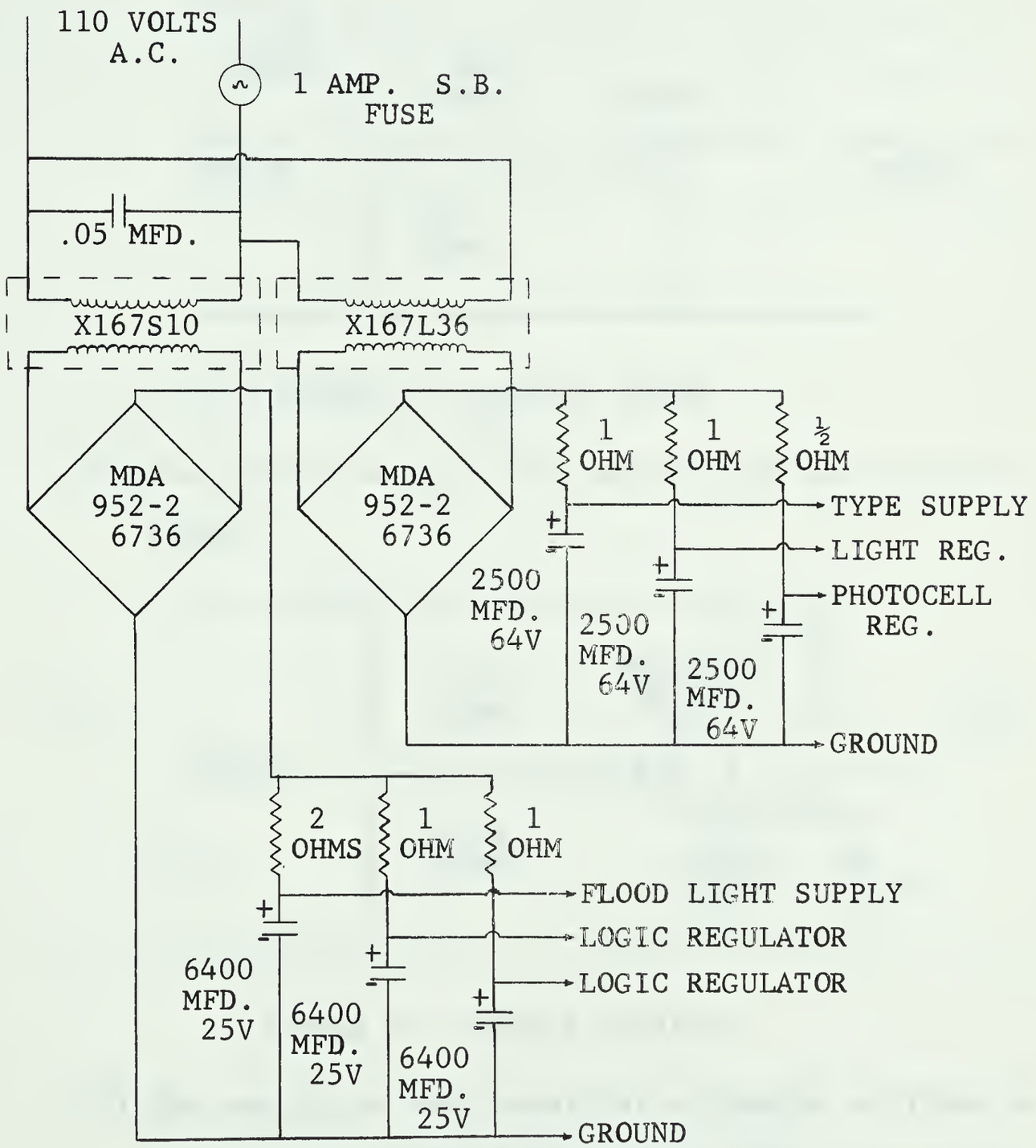


FIGURE 24 D.C. SOURCE SUPPLY

The following supplies are derived from the 50 volt R-C filtered sources:

(1) The 40 volt supply to the photocells utilizes a transistor circuit arranged as shown to clamp the voltage at 40 volts.

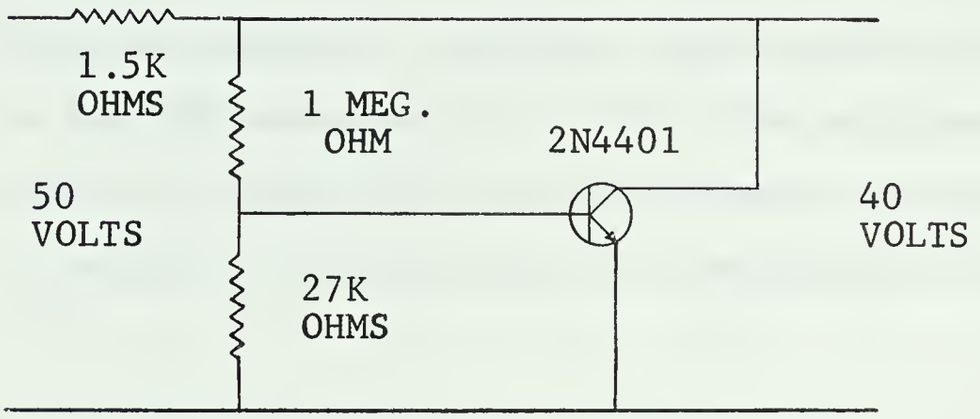


FIGURE 25 VOLTAGE CLAMP

(2) The 28 volt supply is obtained from the circuit shown.

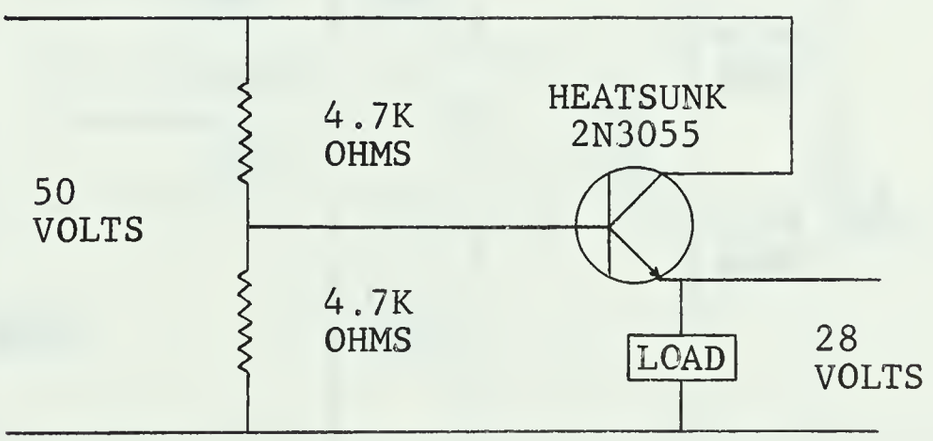


FIGURE 26 VOLTAGE DIVIDER

(3) The supply to the typewriter solenoids utilizes a series resistance of 75 ohms to limit the steady state current through the solenoids.

The following supplies are derived from the 14 volt R-C filtered sources:

(1) The 10 volt supply to the photocell flood bulb in the handboard uses the series resistance of the R-C filter to obtain the desired voltage.

(2) The 3.6 volt supplies to the logic are obtained from two regulator networks. Each network uses an L.M.100 power regulator IC. The peripheral transistors and the circuitry shown are necessary to obtain 3.6 volts with a 2.5 amp current limit.

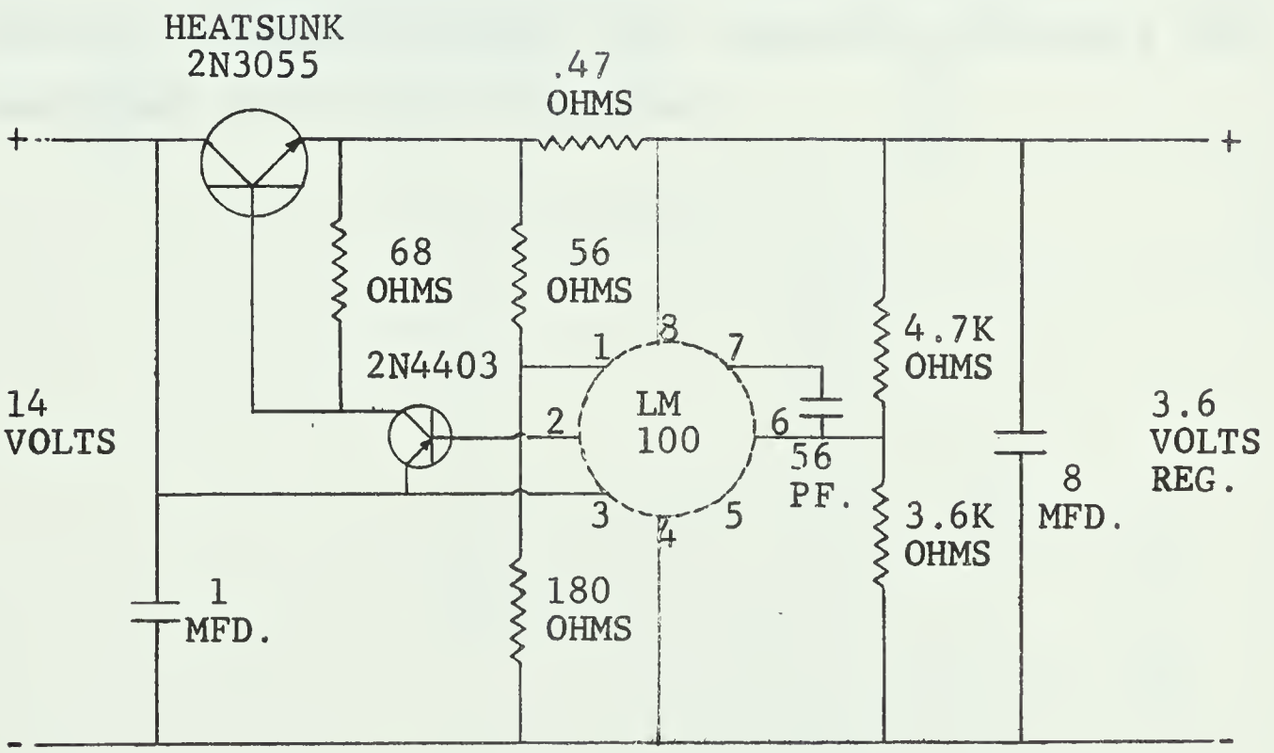


FIGURE 27 LOGIC SUPPLY REGULATOR

LIGHTBOARD

FIGURE 28 shows an exploded view of the lightboard. This board is designed around sixty-six lightbulb sockets which plug into the aluminium sheet. The sheet is supplied with 28 volts and is insulated from the outer cabinet by the sectional facing. This facing also divides the board into 2½" cellular units. A lightbulb is centered in each cell and the "pigtail" from each bulb is wired to a cross-connect board. The cross-connect board is connected by cable and plug to the console. The front face of the lightboard is made of frosted plexiglass in order to diffuse the light. The typewriter functions are stencilled in the positions shown.

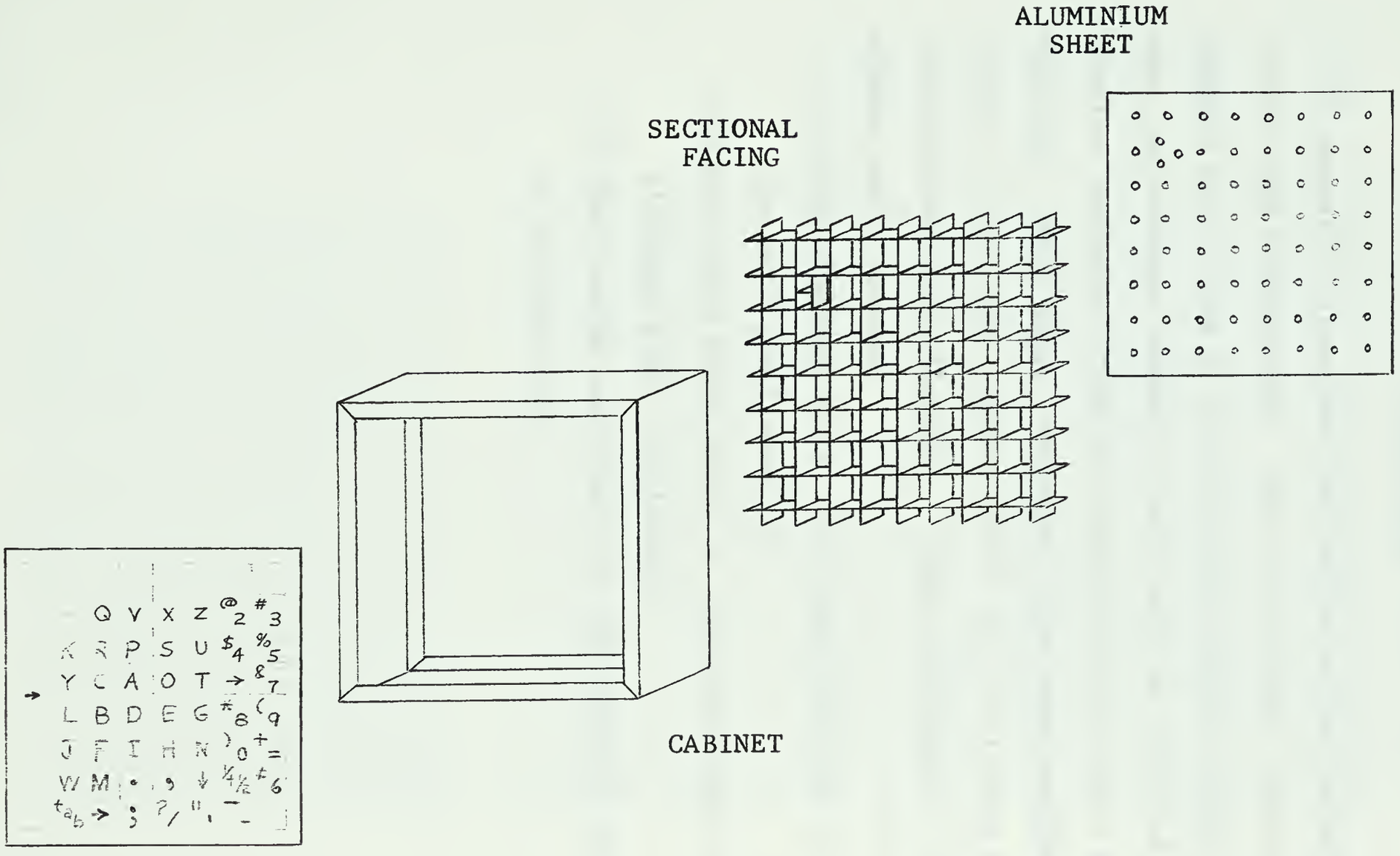


FIGURE 28 LIGHTBOARD

CONCLUSION

A versatile interface unit which allows paraplegics to type was constructed. The unit and the "switches" developed are in use at the Glenrose Hospital School. However, an enormous amount of work will be required to synthesize "switches" that are compatible with each patient's handicap. When these "switches" have been designed and proven, a much more sophisticated unit utilizing a small computer may prove feasible. Some advantages of this system would include:

(1) Time sharing would allow many patients to utilize the unit simultaneously.

(2) Operating modes would be under soft ware control, allowing great flexibility.

(3) Whole words could make up one function indicated on a visual aid.

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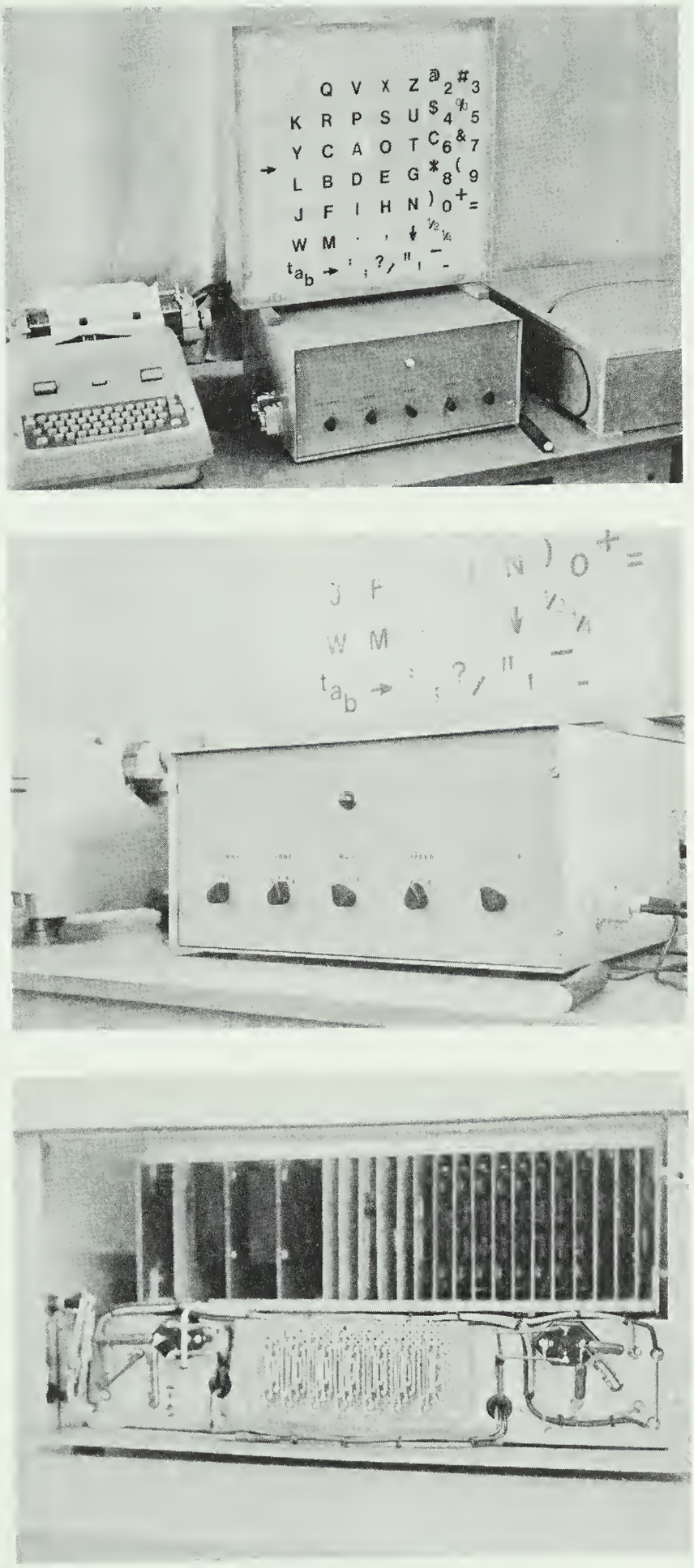

FIGURE 29 VIEWS OF MITOP